Please add new claim 21, as follows:

--21. (New) The semiconductor device of claim 1 wherein the seed layer and the dielectric layer combine to cover the seed separating layer.--

REMARKS

This paper is filed in response to the office action mailed on August 5, 2002.

In the office action, the restriction requirement is made and, accordingly, applicant cancels claims 13-20, without prejudice or disclaimer.

Claim 1 has been amended; claim 21 has been added; claims 1-12 and 21 are pending.

The office action rejects the claims under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,923,062 ("Ohno") or as being obvious under 35 U.S.C. § 103 in view of Ohno in combination with either U.S. Patent No. 6,407,422 ("Asano") or U.S. Patent No. 6,218,259 ("Akram"). In response, claim 1 has been amended to traverse these rejections. Further, the specification has been amended to provide clear antecedent basis for the new language of amended claim 1. Applicant respectfully submits that no new matter is added in light of the fact that all amendments to claim 1 and the specification are fully supported by the original specification and drawings.

The Patent Office's anticipation reference, Ohno, also serves as its base reference for both obviousness rejections. However, the structure of Ohno is clearly different from the structure recited by amended claim 1. The alleged seed separating layer 314 is not disposed beneath any portion of a seed layer. As clearly shown in Fig. 3 of Ohno, the layer 314 is disposed laterally between the lower electrode layer 313b and the dielectric layer 315 and is sandwiched between the lower electrode layer 313a and the insulating layer 310.

In contrast, amended claim 1 recites a structure wherein the seed separating layer is partially covered by the seed layer and partially covered by the dielectric medium. This structure prevents any contact between the dielectric medium 51 and the connecting part 44 as shown in Figs. 3D and 4 of the specification. Specifically, even if misalignment occurs as shown in Fig. 4, the dielectric medium 51 is still prevented from contact with the connecting part 44 by at least the seed layer 46 and, as shown in Fig. 3D, without any misalignment, the dielectric medium 51 is prevented

from coming into contact with the connecting part 44 by both the seed separating layer 45 and the seed layer 46.

In contrast, in order to prevent the dielectric layer 315 from coming into contact with the connecting part 312, Ohno relies upon electrodes 313a and 313b with a large surface area as compared to the surface area of the contact hole 311 and connecting part or plug 312. Obviously, the design of Ohno does not lend itself to increased miniaturization or future design rules. In any event, Ohno fails to teach or suggest the structure of claim 1 in that no portion of the lower electrode 313b covers any portion of the layer 314 and no portion of the dielectric layer 315 covers the layer 314.

Thus, Ohno does not anticipate claim 1 and, accordingly, cannot serve as a base reference for an obviousness rejection of claim 1 given the fact that neither Asano nor Akram disclose a combination of the seed separating layer, seed layer and dielectric layer required by amended claim 1.

Accordingly, applicant respectfully submits that the rejection of claims 1-3, 5, 7 and 9-12 under 35 U.S.C. § 102(b) as being anticipated by Ohno is improper and should be withdrawn. Further, applicant respectfully submits that the rejection of claims 4 and 6 under 35 U.S.C. § 103 as being unpatentable over Ohno in view of Asano is improper and should be withdrawn. Finally, applicant respectfully submits that the rejection of claim 8 under 35 U.S.C. § 103 as being unpatentable over Ohno in view of Akram is improper and should be withdrawn.

Applicant respectfully submits that all claims are now in a condition for allowance and an early action so indicating is respectfully requested.

The Commissioner is authorized to charge any fee deficiency required by this paper, or credit any overpayment, to Deposit Account No. 13-2855.

Respectfully submitted,

MARSHALL, GERSTEIN & BORUN
6300 Sears Tower
233 South Wacker Drive
Chicago, Illinois 60606-6357
(312) 474-9577

October 16, 2002 By:

Michael R. Hull
Reg. No. 35,902

VERSION WITH MARKINGS TO SHOW CHANGES

In the Specification:

The paragraph beginning on page 10, line 1, has been replaced with the following rewritten paragraph:

-- Then the capacitor sacrificial film 47 is etched until the surface of the seed separating layer 45 is exposed. Thus, the portions of the seed layer 46 where the lower electrode 50 has not been deposited are exposed. Then the exposed portions of the seed layer 46 are removed by etching. Under this condition, the seed layer 46 is separated into a plurality of parts, and therefore, the lower electrode 50 is also separated into a plurality of parts between adjacent cells. Further, as shown in Fig. 3C, part of the seed layer 46 disposed beneath the electrode 50 still covers an inner portion of the seed separating layer 45 that encircles the connecting part 44.--

The paragraph beginning on page 10, line 19 has been replaced with the following rewritten paragraph:

-- Then upon the entire surface including the lower electrode 50, there are sequentially deposited a dielectric medium 51 and an upper electrode 52. The dielectric medium 51 covers the remaining portion of the seed separating layer 45 not covered by the seed layer 46.--

The paragraph beginning on page 11, line 21 has been replaced with the following rewritten paragraph:

-- As shown in the drawing, the completed semiconductor device includes: a connecting part 44 connected through an insulating layer 43 of a substrate 41 to a conductive layer 42; a seed separating layer 45 formed around the connecting part 44 and the insulating layer 43 to open at least the connecting part 44; a seed layer 46 filled into the open part of the seed separating layer 45 and covering an inner portion of the seed separating layer 45; and a capacitor consisting of: a lower electrode 50 formed upon the seed layer 46, a dielectric medium 51 formed upon the lower electrode 50 and the remaining portion of the seed separating layer 45 not covered by the seed layer 46, and an upper electrode 52 formed upon the dielectric medium 51.--

In the Claims:

Claim 1 has been amended, as follows:

1. (Amended) A semiconductor device comprising:

a substrate coated with an insulating layer;

a connecting part connected to a conductive layer through the insulating layer of the substrate;

a seed separating layer formed around the connecting part and the insulating layer, the seed separating layer defining [to provide] an open region that exposes at least part of the connecting part;

a seed layer disposed in the open region of the seed separating layer and covering a first portion of the seed separating layer; and

a capacitor comprising a lower electrode formed on the seed layer, a dielectric medium formed on the lower electrode and further covering a second portion of the seed separating layer, and an upper electrode formed on the dielectric medium.

Claims 13-20 have been canceled without prejudice or disclaimer.

Claim 21 has been added, as follows:

--21. (New) The semiconductor device of claim 1 wherein the seed layer and the dielectric layer combine to cover the seed separating layer.--